CARRIER FREQUENCY COMPENSATION SYSTEM AND METHOD

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ABSTRACT OF THE DISCLOSURE

A radio modem for use in a communications system monitors an error signal generated by the modem's phase-locked loop (PLL) used to demodulate an IF frequency signal and recover a digital data signal. If, due to long-term drift of a reference oscillator of the receiver or due to transmitter frequency drift, the PLL error signal exceeds a predetermined value typically corresponding to 75% of its hold-in or lock maintenance range, a carrier frequency compensation process is initiated to recenter the PLL on the current IF signal by reprogramming a frequency synthesizer supplying the PLLs input signal. A CPU causes the frequency synthesizer to increment or decrement the frequency of the signal provided to the PLL to bring the operating frequency of the PLL closer to that of the IF signal. If the required frequency compensation falls outside the tuning range of the receiving modem, either because the frequency synthesizer is unable to generate the required frequency or because of excessive shift of the IF frequency, then the receiver terminal negotiates with the corresponding transmitter terminal to converge both IF frequencies. As a result, the transmitter changes its frequency by an amount equal to one-half of the required frequency shift while the receiver terminal performs the remainder of the frequency shift. Upon reprogramming of one or both synthesizers to readjust the operating frequencies of the receiver and/or transmitter, the receiver performs a search process to reacquire lock on the transmitter, starting at the predicted IF center frequency and alternately scanning in increasing amounts away from and on either side of the predicted center frequency until a signal lock is achieved or until a timeout occurs.